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TO EXAMINER: Mai, Tan V. **FAX #:** 571-273-3726

GROUP ART UNIT: 2193 .

ADDRESS: U.S. Patent and Trademark Office

P.O. Box 1450, Alexandria, VA 22313-1450

EXAMINER PHONE: 571-272-3726

Transmitted here with regarding Attorney docket no. 800.0117, Application Serial No. 10/799,316, Filed March 12, 2004, are the following:

Information copy of Amendment After Final filed August 11, 2008.

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TRANSMITTAL FORM		
	Application Number	10/799 316
	Filing Date	Mar 12, 2004
	First Named Inventor	Pitsoros, Nikos P
	Art Unit	2183
(to be used for all correspondence after initial filing)	Examiner Name	Mai, Tan V.
Total Number of Pages in This Submission	Attorney Docket Number	800.0117 A01550

ENCLOSURES *(Check all that apply)*

- [X] Fee Transmittal Form
  - [ ] Fee Attached
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  - [ ] Affidavits/declaration(s)
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- [ ] Information Disclosure Statement
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Firm Name	Priest & Goldstein, PLLC		
Signature	*[signature]*		
Printed name	Peter H. Priest		
Date	August 11, 2008	Reg. No.	30210

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TRANSMITTAL FORM

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Total Number of Pages in This Submission

Application Number	10/799,316
Filing Date	Mar 12, 2004
First Named Inventor	Pitsianis, Nikos P.
Art Unit	2193
Examiner Name	Mai, Tan V.
Attorney Docket Number	800.0117 A01559

ENCLOSURES *(Check all that apply)*

- [X] Fee Transmittal Form
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- [X] Amendment / Reply
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Priest & Goldstein, PLLC		
Signature			
Printed name	Peter H. Priest		
Date	August 11, 2008	Reg. No.	30210

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Typed or printed name	Marianna Tortorelli	Date	August 11, 2008

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800.0117
A01559

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Pitsianis et al.
Serial No.:	10/799,316
Filed:	March 12, 2004
For:	METHODS AND APPARATUS FOR SINGLE STAGE GALOIS FIELD OPERATIONS
Group:	2193
Examiner:	Mai, Tan V.

Durham, North Carolina
August 8, 2008

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Amendment Transmittal

Sir:

1. Transmitted herewith is an Amendment for the above-identified application, responsive to an Office Action dated June 18, 2008.

FEE FOR CLAIMS AS AMENDED

2. [X] No additional fee is required.

   [ ] The additional fee has been calculated as shown below:

CLAIMS AS AMENDED

	Claims Remaining After Amendment		Highest No. Previously Paid For	Present Extra	Rate		Additional Fee
Total Claims	14	-	20	0	x $50.00	=	0.00
Independent Claims	3	-	6	0	x $210.00	=	0.00
Multiple Dependent Claims		-			x $360.00	=	
						TOTAL	0.00

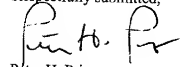
3. [ ] Enclosed is our check for $ _____ to cover the filing fee.

[ ] Charge the fee of $ _____ to Credit Card (see attached form).

[ ] Charge the fee of $ 120 for a 1 month extension of time to Credit Card (see attached form). This letter petitions for a 1 month extension of time to respond.

4. [X] The Commissioner is hereby authorized to charge any additional fees which may be required for this amendment, including any fee for extension of time or credit any overpayment to Law Offices of Peter H. Priest **Deposit Account No. 50-1058.**

Respectfully submitted,



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A01559

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Pitsianis et al.

Serial No.: 10/799,316

Filed: March 12, 2004

For: METHODS AND APPARATUS FOR SINGLE STAGE GALOIS FIELD OPERATIONS

Group: 2193

Examiner: Mai, Tan V.

Durham, North Carolina
August 11, 2008

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Amendment After Final

Sir:

In response to the final Official Action of June 18, 2008, please amend the above identified application as follows:

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method for Galois field ($GF(2^m)$) multiplication by a logic circuit, where m is a positive integer, and the $GF(2^m)$ multiplication operation calculates the multiplication of two polynomials producing a product which is divided by a generator polynomial, and wherein the multiplication of the two polynomials is combined with the division operation whereby the $GF(2^m)$ multiplication is computed as a single function $GF(2^m)$ multiplication operation, the method comprising:

generating x^{m-i} polynomial coefficient terms from multiplication and division mathematical operations, where i is a variable;

combining x^{m-i} polynomial coefficient terms having the same exponents from the multiplication and division mathematical operations to generate a recurrence relation that represents the combination of the multiplication and division operations;

computing the recurrence relation using the combined x^{m-i} polynomial coefficient terms in the single function $GF(2^m)$ multiplication operation to produce a $GF(2^m)$ result; and

storing the $GF(2^m)$ result in memory in a computer readable form.

2. (previously presented) The method of claim 1 wherein the recurrence relation for the single $GF(2^m)$ multiplication function is $Y(i) = Y(i-1) + (q_{m-i}*p + Y(i-1)_{2m-1}*g)*x^{m-i}$, i=1,

2, …, m and where Y(0) = 0, Y(i=m) is the GF(2^m) result, p and q are coefficients of input polynomials p[x] and q[x], respectively, and g is the coefficients of a generator polynomial g[x].

3. (previously presented) The method of claim 1 further comprising:

computing the recurrence relation for a single GF(2^m) multiplication function as $Y(i) = Y(i-1) + (q_{m-i}*p + Y(i-1)_{2m-1}*g\ Y(i-1)_{m-1}*g)*x^{m-i}$, i=1, 2, …, m and where Y(0) = 0, Y(i=m) is the GF(2^m) result, p and q are coefficients of input polynomials p[x] and q[x], respectively, and g is the coefficients of a generator polynomial g[x] in an m by m single function computation array utilizing m bits per internal calculation stage

4. (currently amended) A method for Galois field (GF(2^m)) multiplication by a logic circuit, where m is a positive integer, and the GF(2^m) multiplication operation calculates the multiplication of two polynomials producing a product which is divided by a generator polynomial, and wherein the multiplication of the two polynomials is combined with the division operation whereby the GF(2^m) multiplication is computed as a single function GF(2^m) multiplication operation, the method comprising:

generating x^{m-i} polynomial coefficient terms from multiplication and division mathematical operations, where i is a variable;

combining x^{m-i} polynomial coefficient terms having the same exponents from the multiplication and division mathematical operations to generate a recurrence relation that represents the combination of the multiplication and division operations;

computing the recurrence relation using the combined x^{m-i} polynomial coefficient terms in the single function $GF(2^m)$ multiplication operation thereby calculating m by m bits for the $GF(2^m)$ multiplication function to produce an m bit $GF(2^m)$ result; and

storing the m bit $GF(2^m)$ result in memory in a computer readable form.

5. (previously presented) The method claim 4 wherein the the recurrence relation for the single $GF(2^m)$ multiplication function is $Y(i) = Y(i-1) + (q_{m-i}*p + Y(i-1)_{m-i}*g)*x^{m-i}$, i=1, 2, …, m and where $Y(0) = 0$, $Y(i=m)$ is the m bit $GF(2^m)$ result, p and q are coefficients of input polynomials p[x] and q[x], respectively, and g is the coefficients of a generator polynomial g[x].

6. (previously presented) The method of claim 4 wherein the step of computing the recurrence relation is accomplished in an m by m single function computation logic array utilizing m bits per internal logic stage.

7. (previously presented) A GF multiplication circuit cell producing result $Y(i)_j$ for $i \in \{1, 2, \ldots, m\}$, $j \in \{0, 1, \ldots, m-1\}$, where m is a positive integer, and a selected i and j value comprising:

a bit q_{m-i} selected from the set $\{q_{m-1}, q_{m-2}, \ldots, q_{m-i}, \ldots, q_0\}$ of first product inputs based on the selected i value;

a bit p_j selected from the set $\{p_{m-1}, p_{m-2}, \ldots, p_j, \ldots, p_0\}$ of second product inputs based on the selected j value;

a bit g_j selected from the set $\{g_{m-1}, g_{m-2}, \ldots, g_j, \ldots, g_0\}$ of generator polynomial coefficients based on the selected j value;

a most significant bit $Y(i-1)_{m-1}$ of a previous stage of GF multiplication circuit cells results;

a value of the rightmost neighbor bit $Y(i-1)_{j-1}$ of a previous stage of GF multiplication circuit cell results, wherein the rightmost neighbor bit $Y(i-1)_{j-1}$ is in relation to the present GF multiplication circuit cell producing result $Y(i)_j$ for the selected i and j values;

a logic device producing q_{m-i} AND p_j as output A;

a logic device producing $Y(i-1)_{m-1}$ AND g_j as output B; and

a logic device producing A XOR B XOR $Y(i-1)_{j-1}$ as result $Y(i)_j$ to be utilized in one or more GF multiplication circuit cells or stored in a processor accessible storage unit.

8. (previously presented) The GF multiplication circuit cell of claim 7 disposed within an m-by-m array of interconnected GF multiplication circuit cells for producing a Galois Field (2^m) multiplication result Y, where m is a positive integer, further comprising:

input operand $q = (q_{m-1}\ q_{m-2} \ldots q_0)$;

input operand $p = (p_{m-1}\ p_{m-2} \ldots p_0)$;

input operand $g = (g_{m-1}\ g_{m-2} \ldots g_0)$;

the $Y(i-1)_{m-1}$ and the $Y(i-1)_{j-1}$ array border GF multiplication circuit cell input values set to 0; and

output Y result which is stored in a computer readable form.

9. (original) The GF multiplication circuit cell of claim 8 wherein the m-by-m array of interconnected GF multiplication circuit cells further comprises:

the interconnections of the GF multiplication circuit cells governed by the equation

$Y(i) = Y(i-1) + (q_{m-i}*p + Y(i-1)_{m-1}*g)*x^{m-i}$, i=1, 2, …, m and where $Y(0) = 0$.

10. (original) The GF multiplication circuit cell of claim 8 wherein the m-by-m array of GF multiplication circuit cells is further disposed within a grouping of multiple m-by-m arrays in a processor execution unit and further comprises:

a GF (2^m) multiplication instruction with a data type field specifying at least one GF (2^m) multiplication operation; and

means for connecting the multiple m-by-m arrays inputs and outputs for performing at least one GF (2^m) multiplication in the execution of the GF (2^m) multiplication instruction.

11. (original) The GF multiplication circuit cell of claim 8 wherein the input operands $q = (q_{m-1}\ q_{m-2}\ \dots\ q_0)$, $p = (p_{m-1}\ p_{m-2}\ \dots\ p_0)$, and $g = (g_{m-1}\ g_{m-2}\ \dots\ g_0)$ are connected to read outputs of at least one storage unit in a processor system.

12. (original) The GF multiplication circuit cell of claim 8 wherein the output Y results are connected to at least one storage unit write inputs in a processor system.

13. (original) The GF multiplication circuit cell of claim 11 wherein the at least one storage unit is a processor accessible register file.

14. (original) The GF multiplication circuit cell of claim 12 wherein the at least one storage unit is a processor accessible register file.

15-19. (canceled)

Remarks

The present amendment responds to the final Official Action dated June 18, 2008. That Action rejected claims 1-14 under 35 U.S.C. § 101. This sole ground of rejection is addressed below. Claims 1 and 4 have been amended to be more clear and distinct. Claims 15-19 have been previously canceled without prejudice confirming a previous election. Claims 1-14 are presently pending.

Interview Summary

The Examiner is thanked for the courtesy of a brief telephone interview to clarify the Section 101 objection. It was agreed that claim 1 would be amended to recite additional hardware structure for performing the method, and that claim 7 which already recites a "multiplication circuit cell" and multiple logic devices would be reconsidered.

Section 101 Rejection

The final Official Action again suggested that claims 1-14 disclose steps/elements of performing mathematical functions without disclosing a practical application with a concrete, useful, and tangible result.

As noted at page 1, lines 10 and 11, a Galois field "multiplication of two input elements is an important function which signal processing units and DSPs may need to perform." As further discussed at page 2, lines 1-7, a variety of potential approaches to such multiplication exist and the listed patents further discuss practical applications for the calculations as does the Summary of the Invention at page 2, lines 9-11. The presently claimed improved approaches to

such calculations are not divorced from the structure employed to perform them and are clearly patentable subject matter under Section 101.

More particularly, claims 1 and 4 have now been amended to recite that the method for Galois field multiplication is performed "by a logic circuit" in addition to the result being stored "in memory in a computer readable form." Claim 7 recites a "GF multiplication circuit cell" and multiple logic devices. Such subject matter is clearly statutory.

Conclusion

As no art rejections have been made, withdrawal of the present rejection and prompt allowance are requested.

Respectfully submitted,

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